

IN THE CLAIMS

Claims 1-33 (cancelled).

34. (currently amended) An intermediary of a semiconductor device comprising:

a semiconductor substrate formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate;

a pillar region comprised of a plurality of pillars comprising a dielectric material formed in the first recessed region and extending from the lower surface, wherein a plurality of voids ~~region~~ is ~~formed~~ within the pillar region; and

a polysilicon cap layer having a ~~lower~~ surface formed adjoining upper surfaces of the pillar region and overlying each of the plurality of pillars, wherein the ~~lower~~ surface of the polysilicon cap layer is aligned with each of the plurality of voids ~~region~~, and wherein sidewall surfaces of the plurality of pillars ~~region~~ are devoid of the polysilicon cap layer, and wherein the pillar region and the polysilicon cap layer ~~and the void region~~ are configured to form an isolation region having reduced substrate capacitance.

35. (previously presented) The intermediary of claim 34, wherein the polysilicon cap layer has a thickness of about 4,500 angstroms.

36. (previously presented) The intermediary of claim 34, wherein the upper surfaces of the pillar region are

recessed below the major surface of the semiconductor substrate.

37. (previously presented) The intermediary of claim 36, wherein the upper surfaces are recessed a distance of about 0.5 microns.

38. (previously presented) The intermediary of claim 34, wherein the pillar region comprises deposited silicon dioxide.

39. (currently amended) The intermediary of claim 34, wherein the pillar region comprises a matrix of a plurality of pillars.

40. (previously presented) The intermediary of claim 39, wherein at least a portion of the matrix of pillars includes pillars having a generally rectangular shape.

41. (currently amended) The intermediary of claim 34, ~~wherein the pillar region comprises a contiguous matrix~~ wherein the polysilicon cap layer is aligned with each of the plurality of voids without completely overlying each of the plurality of voids.

42. (currently amended) The intermediary of claim 34, wherein the pillar region extends a distance of about 4.5 micrometers from the lower surface of the first recessed region and has a dielectric constant of about 3.5.